Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended): A thin film transistor substrate for a liquid crystal display, comprising:

a data line extending in a first straight line direction;

a gate line extending in a second straight line direction;

a source electrode connected to [[a]] the data line so as to receive video data;

a drain electrode opposed to the source electrode;

a channel between the drain electrode and the source electrode, wherein the channel has a desired size; and

a gate electrode extending from [[a]] the gate line for opening and closing the channel, wherein the gate electrode includes a head portion ~~having at least one side inclined at a predetermined angle~~, the head portion having an inclined part sloped at a first angle relative to the first straight line direction of the data line and a second angle relative to the second straight line direction of the gate line, the inclined part being unparallel to the gate line.

2. (Previously Presented): The thin film transistor substrate as claimed in claim 1, wherein the head portion is inclined parallel to a rubbing direction.

3. (Previously Presented): The thin film transistor substrate as claimed in claim 1, wherein the head portion is inclined between about 35° to 45° from the longitudinal direction of the gate electrode.

4. (Original): The thin film transistor substrate as claimed in claim 1, wherein the gate electrode includes a concave neck, and wherein the concave neck reduces overlap of the drain electrode and the gate electrode.

5. (Previously Presented): The thin film transistor substrate as claimed in claim 4, wherein the concave neck is narrower than a maximum width of the head by less than about 5μm.

6. (Original): The thin film transistor substrate as claimed in claim 1, further comprising:

a gate insulating film on the substrate and over the gate electrode;

a semiconductor layer on the gate insulating film and over the gate electrode;

a protective layer over the gate insulating film and over the source and drain electrodes; and

a pixel electrode on the protective layer and connected to the drain electrode;

wherein the source and drain electrodes are on the semiconductor layer.

7. (Previously Presented): The thin film transistor substrate as claimed in claim 6, wherein the pixel electrode is formed with an edge that follows the inclination of the head portion, and wherein the pixel electrode further corresponds with the concave neck of the gate electrode.

8. (Previously Presented): The thin film transistor substrate as claimed in claim 1, further comprising:

a gate insulating film on the substrate and gate electrode;

an active layer and an ohmic contact layer over the gate insulating film, wherein the active layer and the ohmic contact layer overlap the gate electrode;

a protective layer over the gate insulating film and patterned to match the active layer; and

a pixel electrode on the protective layer and connected to the drain electrode;

wherein the source and drain electrodes are pattern to match the ohmic contact layer.

9. (Previously Presented): The thin film transistor substrate as claimed in claim 8, wherein the pixel electrode is formed with an edge that follows the inclination of the head portion, and wherein the pixel electrode further corresponds with the concave neck of the gate electrode.

10. (Previously Presented): The thin film transistor substrate as claimed in claim 1, further comprising:

a gate insulating film on the substrate and over the gate electrode;

a semiconductor layer on the gate insulating film and over the gate electrode;

a protective layer on the gate insulating film and over the source and drain electrodes; and

a pixel electrode on the protective layer and connected to the drain electrode;

wherein the source and drain electrodes correspond with the semiconductor layer.

11. (Previously Presented): The thin film transistor substrate as claimed in claim 10, wherein the pixel electrode is formed with an edge that follows the inclination of the head, and wherein the pixel electrode further corresponds with the concave neck of the gate electrode.

12. (Withdrawn): A method of fabricating a thin film transistor substrate, comprising the steps of :

forming a gate metal layer on a substrate; and

patterning the gate metal layer to form a gate electrode having a head portion with at least one side inclined at a desired angle.

13. (Withdrawn): The method as claimed in claim 12, further comprising the steps of:

forming a gate insulating film on the substrate and over the gate electrode;

forming a semiconductor layer on the gate insulating film;

forming source and drain electrodes on the semiconductor layer so as to define a channel;

forming a protective layer on the gate insulating film and over the source and drain electrodes; and

forming a pixel electrode on the protective layer.

14. (Withdrawn): The method as claimed in claim 12, further comprising the steps of

forming a gate insulating film on the substrate in such a manner as to cover the gate electrode;

depositing first and second semiconductor layers and a metal layer on the gate insulating film;

patterning the metal layer and the second semiconductor layer to form source and drain electrodes;

providing a protective material layer on the first semiconductor layer in such a manner as to cover the source and drain electrodes, patterning the first semiconductor layer and the protective layer material to form a protective layer and a semiconductor pattern; and

forming a pixel electrode on the protective layer.

15. (Withdrawn): The method as claimed in claim 12, further comprising the steps of:

forming a gate insulating film and a semiconductor material on the substrate in such as a manner to cover the gate electrode;

forming source and drain electrodes on the semiconductor material;

depositing a protective layer material on the gate insulating film in such a manner as to cover the source and drain electrodes, simultaneously patterning the semiconductor material and the protective layer material to form a semiconductor pattern and a protective layer; and

forming a pixel electrode on the protective layer.

16. (Withdrawn): The method as claimed in claim 12, further comprising the steps of forming a gate electrode having a head portion inclined parallel to a rubbing direction of the thin film transistor substrate.

17. (Withdrawn): The method as claimed in claim 16, further comprising the steps of forming a gate electrode having a neck portion that is narrower than a maximum width of the head portion by less than about 5 μm.

18. (Withdrawn): The method as claimed in claim 17, further comprising the steps of:

forming a gate insulating film over the gate electrode;

forming a semiconductor layer on the gate insulating film; and

forming source and drain electrodes on the semiconductor layer so as to define a channel.

19. (Withdrawn): The method as claimed in claim 18, further comprising the steps of providing a protective material layer on the semiconductor layer.

20. (Withdrawn): The method as claimed in claim 19, further comprising the steps of forming a pixel electrode on the protective layer.

21. (New): A thin film transistor substrate for a liquid crystal display, comprising:

a data line extending in a first straight line direction, the data line receiving video data;

a gate line extending in a second straight line direction, the gate line being perpendicular to the data line;

a source electrode extending from the data line in a same direction as the gate line;

a drain electrode opposite the source electrode;

a semiconductor layer having a channel, the channel being located between the drain electrode and the source electrode; and

a gate electrode extending from the gate line and in a same direction as the data line, a portion of the source electrode overlapping the gate electrode and a portion of the drain electrode overlapping the gate electrode, and

wherein a first overlapping portion between the source electrode and the gate electrode has a first width and a second overlapping portion between the drain electrode and the gate electrode has a second width, the first width being larger than the second width, the first width of the source electrode and the second width of the drain electrode corresponding to a shape of the semiconductor layer;

whereby the shape of the gate electrode reduces the overlapping areas between the gate electrode and the source and drain electrodes to reduce a parasitic capacitance.

22. (New): The thin film transistor substrate as claimed in claim 21, wherein the gate electrode includes a head portion having at least one side inclined at a predetermined angle and the head portion is inclined parallel to a rubbing direction.

23. (New): The thin film transistor substrate as claimed in claim 22, wherein the head portion is inclined between about 35° to 45° from the longitudinal direction of the gate electrode.

24. (New): The thin film transistor substrate as claimed in claim 21, wherein the gate electrode includes a concave neck, and wherein the concave neck reduces overlap of the drain electrode and the gate electrode.

25. (New): The thin film transistor substrate as claimed in claim 24, wherein the concave neck is narrower than a maximum width of the head by less than about 5 μm.

26. (New): The thin film transistor substrate as claimed in claim 1, wherein the semiconductor layer has a shape of a funnel having a top portion and a bottom portion, the first overlapping portion between the source electrode and the gate electrode corresponding to the top portion of the funnel and the second overlapping portion between the drain electrode and the gate electrode corresponding to the bottom portion of the funnel.

27. (New): The thin film transistor substrate as claimed in claim 26, wherein the semiconductor layer includes an amorphous semiconductor layer and a doped amorphous semiconductor layer.

28. (New): The thin film transistor substrate as claimed in claim 1, wherein the channel is part of a semiconductor layer having a shape of a funnel having a top portion and a bottom portion, an overlapping portion between the source electrode and the gate electrode corresponding to the top portion of the funnel and an overlapping portion between the drain electrode and the gate electrode corresponding to the bottom portion of the funnel.

29. (New): The thin film transistor substrate as claimed in claim 28, wherein the semiconductor layer includes an amorphous semiconductor layer and a doped amorphous semiconductor layer.

30 (New): The thin film transistor substrate as claimed in claim 1, wherein the first angle and the second angle are different.

31. (New): A thin film transistor substrate for a liquid crystal display, comprising:

a data line and a gate line defining a pixel area;

a source electrode extending from the data line;

a drain electrode opposite the source electrode;

a semiconductor layer having a channel, the channel being located between the drain electrode and the source electrode; and

a gate electrode extending from the gate line, the gate electrode having means for reducing the overlapping areas between the gate electrode and the source and drain electrodes, whereby a parasitic capacitance is reduced.